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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HARKNESS, CHARLES A	

ART UNIT	PAPER NUMBER
2183	3

DATE MAILED: 11/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/746,796	COHEN ET AL.	
	Examiner	Art Unit	
	Charles A Harkness	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☒ Claim(s) *16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Papers Submitted

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Change of Address as received on 08/16/01.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

3. The applicant or their representatives are urged to review the specification and submit corrections for all mistakes of a grammatical, clerical, or typographical nature.

Claim Objections

Claim 16 is objected to for the following reasons: Since the Java Virtual Machine is a common term in the art, and is known as a software-based "computer", and is not a real computer but exists only in software (as defined by the Microsoft Computer Dictionary Fourth Edition) the circuit claimed can not be a part of the Java Virtual Machine.. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-6, 8-9, 12-14, and 17-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Hilgendorf et al, U.S. Patent Number 5,925,124 (herein referred to as Hilgendorf).

5. Referring to claim 1 Hilgendorf has taught an apparatus comprising:

a circuit configured to translate instruction codes of a first instruction set into sequences of instruction codes of a second instruction set that emulate a functionality of the instruction codes of the first instruction set (Hilgendorf abstract figures 1 and 2, column 3 lines 8-56).

6. Referring to claim 2 Hilgendorf has taught wherein said sequences of instruction codes of a second instruction set are stored in a computer readable medium (Hilgendorf abstract figures 1 and 2, column 3 lines 8-56, column 7 lines 9-17).

7. Referring to claim 3 Hilgendorf has taught wherein said computer readable medium comprises a microcode memory (Hilgendorf abstract figures 1 and 2, column 3 lines 8-56, column 7 lines 9-17).

8. Referring to claim 4 Hilgendorf has taught wherein said instruction codes of said first instruction set are used to address said microcode memory (Hilgendorf abstract figures 1 and 2, column 3 lines 8-56, column 7 lines 9-30).

9. Referring to claim 5 Hilgendorf has taught wherein addresses into said microcode memory are generated by a look-up-table in response to said instruction codes of said first instruction set (Hilgendorf abstract figures 1 and 2, column 3 lines 8-56, column 7 lines 9-30).

10. Referring to claim 6 Hilgendorf has taught wherein said instruction codes of said second instruction set comprise native instructions of a target processor (Hilgendorf abstract figures 1 and 2, column 3 lines 8-56, column 7 lines 9-17, column 12 lines 17-38; the instructions that are to be executed must be of the same architecture as the host computer).

11. Referring to claim 8 Hilgendorf has taught wherein said microcode memory can be reprogrammed to support different processors (Hilgendorf column 3 lines 45-56, column 4 lines 51-61).

12. Referring to claim 9 Hilgendorf has taught wherein said circuit is configured to format the sequences of instruction codes of said second instruction set according to an opcode format of a processor (Hilgendorf abstract figures 1 and 2, column 3 lines 8-56, column 9 lines 42-59, column 12 lines 17-38; the instructions that are to be executed must be of the same architecture as the host computer).

13. Referring to claim 12 Hilgendorf has taught wherein said circuit comprises a native instruction sequence generator circuit (Hilgendorf abstract figures 1 and 2, column 3 lines 8-56, column 9 lines 42-59, column 12 lines 17-38; the instructions that are to be executed must be of the same architecture as the host computer).

14. Referring to claim 13 Hilgendorf has taught wherein said circuit is coupled between processor and a memory system (Hilgendorf abstract figures 1 and 2, column 3 lines 8-56, column 12 lines 17-38, column 6 lines 54-61; the external instruction comes from memory and the internal instruction is sent on to the execution unit to be processed).

15. Referring to claim 14 Hilgendorf has taught wherein said circuit is configured to (i) directly connect said processor and said memory system during a first state of operation and (ii) during a second state of operation, communicate with said processor as though said circuit was the memory system and communicate with said memory system as though said circuit was the processor (Hilgendorf abstract figures 1 and 2, column 3 lines 8-56, column 12 lines 17-38,

column 6 lines 54-61; the external instruction comes from memory and the internal instruction is sent on to the execution unit to be processed).

16. Referring to claim 17 Hilgendorf has taught an apparatus comprising:

means for translating instruction codes of a first instruction set into sequences of instruction codes of a second instruction set (Hilgendorf abstract figures 1 and 2, column 3 lines 8-56, column 7 lines 9-30);

means for receiving said instructions of said first instruction set (Hilgendorf abstract figures 1 and 2, column 3 lines 8-56, column 12 lines 17-38, column 6 lines 54-61; the external instruction comes from memory and the internal instruction is sent on to the execution unit to be processed); and

means for presenting said instructions of said second instruction set (Hilgendorf column 9 lines 14-19).

17. Referring to claim 18 Hilgendorf has taught a method for on-the-fly translation of instructions of a first instruction set into instructions of a second instruction set comprising the steps of:

(A) receiving an instruction code of said first instruction set (Hilgendorf abstract figures 1 and 2, column 3 lines 8-56, column 12 lines 17-38, column 6 lines 54-61; the external instruction comes from memory and the internal instruction is sent on to the execution unit to be processed);

(B) generating a sequence of: instruction codes of said second instruction set that will emulate said instruction code of said first instruction set using a hardware translator (Hilgendorf abstract figures 1 and 2, column 3 lines 8-56, column 7 lines 9-30); and

(C) presenting said sequence of instruction codes of said second instruction set (Hilgendorf column 9 lines 14-19).

18. Referring to claim 19 Hilgendorf has taught wherein step C comprises the sub-step of:

(C-1) selecting said sequence of instruction codes of said second instruction set from a microcode memory in response to said instruction codes of solid first instruction set (Hilgendorf abstract figures 1 and 2, column 3 lines 8-56, column 7 lines 9-30).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 10, 12, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hilgendorf in view of Martin U.S. Patent Number 4,439,828 (herein referred to as Martin).

20. Referring to claims 10, 11, and 20 Hilgendorf has not taught wherein said circuit is configured to detect optimizable sequences of instruction codes on-the-fly. Martin has taught wherein said circuit is configured to detect optimizable sequences of instruction codes on-the-fly (Martin abstract column 2 lines 20-52). It would have been obvious to one of ordinary skill in the art at the time of the invention to be configured to detect optimizable sequences of instruction codes on-the-fly. Since Martin shows us that one instruction can take the place of two or more instructions, and that this function improves performance (Martin column 2 lines 20-30), by

allowing other locations in the instruction buffer to be open, and by allowing for a single instruction to take the place of multiple instructions, the processor would also save time. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to be configured to detect optimizable sequences of instruction codes on-the-fly to save time in executing.

21. Claims 7 and 15-16 rejected under 35 U.S.C. 103(a) as being unpatentable over Hilgendorf.

22. Referring to claim 7 Hilgendorf has not explicitly taught wherein said target processor is selected from the group consisting of MIPS, ARM, and Motorola 68K. However, Hilgendorf has taught that the translation circuit can translate the first instruction code into many different codes by replacing the translation table's contents (Hilgendorf column 4 lines 51-61). Since the MIPS, ARM, and Motorola 68K are all commonly used processors in the art, one of ordinary skill in the art at the time of the invention would have recognized that one would use this invention to translate a plurality of instructions from one code type to one of the code types of the MIPS, ARM, and Motorola 68K processors. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention would have made the translation table able to translate instruction to a format to one of the MIPS, ARM, or Motorola 68K processors since these processors are commonly used in industry and would be widely available for use in many systems.

23. Referring to claim 15 Hilgendorf has not explicitly wherein said instruction codes of said first instruction set comprise Java bytecodes. However, Hilgendorf has taught that the translation circuit can translate the first instruction code into many different codes by replacing the

translation table's contents (Hilgendorf column 3 lines 45-56, column 4 lines 51-61). Since Java is a commonly used programming language, one of ordinary skill in the art at the time of the invention would have recognized that you could execute Java code on a computer using Hilgendorf's invention, by translating the code to the host's instruction code. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to translate Java code into the host's computer code since Java is a popular and widely used programming language, and many programs would already be written in Java.

24. Referring to claim 16 Hilgendorf has not explicitly wherein said circuit comprises a hardware portion of a Java virtual machine. See the rejection of claim 15 above. Since it would be obvious to translate from Java code to the host computer code, the circuit used would virtually be executing Java code. However, since the Java Virtual Machine is a common term in the art, and is known as a software-based "computer", and is not a real computer but exists only in software (as defined by the Microsoft Computer Dictionary Fourth Edition) the circuit claimed can not be a part of the Java Virtual Machine.

Conclusion

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR 1.111(c).

Hammond et al, U.S. Patent Number 5,638,525 has taught a processor capable of executing programs that contain RISC and CISC instructions.

Kelly et al, U.S. Patent Number 6,199,152 has taught a translated memory protection apparatus for an advanced microprocessor.

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 703-305-7579. The examiner can normally be reached on 8:00 A.M. – 5:30 P.M. with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-7579.

Charles Allen Harkness

Patent Examiner

Art Unit 2183

November 1, 2003

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SUPERVISORY PATENT EXAMINER
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